although specific terms are employed, they are used in a generic and descriptive sense only and not for the purposes of limitation, the scope of the invention being set forth in the following claims.

That which is claimed is:

1. A vertical power metal oxide semiconductor field effect translator (MOSFET) having a low on-resistance and a high temperature range, comprising:

a C-face substrate of silicon carbide having a first conductivity type;

a first layer of silicon carbide positioned to overlie said C-face substrate and having said first conductivity type for forming a drain-drift region;

a second layer of silicon carbide positioned to overlie said first layer and having a second conductivity type, said second layer forming a channel region;

a third layer of silicon carbide positioned to overlie said second layer and having said first conductivity type, said third layer forming a source region;

a trench formed in portions of said source and drain-draft regions and in portions of said channel region;

an insulating layer positioned to overlie said trench;

a gate electrode positioned to overlie said insulating layer;

a source electrode positioned to overlie at least a portion of said source region; and

a drain electrode positioned to overlie at least a portion of said drain region,

and wherein for a predetermined voltage being applied to said drain electrode, said drain-drift region has a thickness less than and a doping level higher than a comparable silicon MOSFET having a similar breakdown voltage for providing a low on-resistance and thereby obtain the predetermined voltage.

2. A MOSFET according to claim 1, wherein said source and drain electrodes comprise nickel.

3. A MOSFET according to claim 1, wherein said gate includes a gate contact formed of metal.

4. A vertical power MOSFET according to claim 1, further comprising a mesa edge termination of said source, said channel, and said drain-drift regions.

5. A vertical power MOSFET according to claim 1, wherein at least one of said regions of silicon carbide has a polytype selected from the group consisting of 3C, 2H, 4H, 6H, and 15R.

6. A vertical power MOSFET according to claim 1, wherein said first conductivity type comprises n-type silicon carbide and said second conductivity type comprises p-type silicon carbide.

7. A vertical power MOSFET according to claim 1, wherein said first conductivity type comprises p-type silicon carbide and said second conductivity type comprises n-type silicon carbide.

8. A vertical power MOSFET according to claim 1, wherein said channel region is doped with aluminum.

9. A vertical power MOSFET according to claim 1, wherein said channel region is doped with boron.

10. A vertical power MOSFET according to claim 1, wherein said channel region has a doping range from 2E15 to 5E18 atoms/cm^3.

11. A vertical power metal oxide semiconductor field effect transistor (MOSFET) having a low on-resistance and a high temperature range, comprising:

a drain region formed of silicon carbide, said drain region having a C-face substrate of silicon carbide of a first conductivity type and a drain-drift region of silicon carbide positioned to overlie said C-face substrate having said first conductivity type;

a channel region positioned to overlie said drain-drift region formed of silicon carbide and having a second conductivity type;

a source region positioned to overlie said channel region and having said first conductivity type;

a source electrode positioned to overlie at least a first portion of said source region;

a drain electrode positioned to overlie at least a first portion of said drain region;

a trench formed in second portions of said source and drain regions and in portions of said channel region; and

a gate electrode positioned to overlie said trench and adjacent said second portions of said source and drain regions and in said portions of said channel region,

and wherein for a predetermined voltage being applied to said drain electrode, said drain-drift region has a thickness less than a doping level higher than a comparable silicon MOSFET having a similar breakdown voltage for providing a low on-resistance and thereby obtain the predetermined voltage.

12. A vertical power MOSFET according to claim 11, further comprising a mesa edge termination of said source, said channel, and said drain-drift regions.

13. A vertical power MOSFET according to claim 11, wherein said first conductivity type comprises n-type silicon carbide and said second conductivity type comprises p-type silicon carbide.

14. A vertical power MOSFET according to claim 11, wherein said first conductivity type comprises p-type silicon carbide and said second conductivity type comprises n-type silicon carbide.

15. A vertical power MOSFET according to claim 11, wherein said channel region is doped with aluminum.

16. A vertical power MOSFET according to claim 11, wherein said channel region is doped with boron.

17. A vertical power MOSFET according to claim 11, wherein said channel region has a doping range from 2E15 to 5E18 atoms/cm^3.

18. A vertical power MOSFET according to claim 11, wherein said trench has a substantially U-shape.

19. A vertical power MOSFET according to claim 11, wherein said trench has a substantially V-shape.

* * * * *